ELECTRICAL ENGINEERING DEPARTMENT
EEL201 DIGITAL ELECTRONIC CIRCUITS
MINOR II

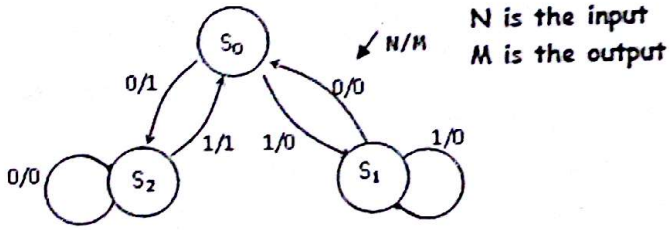
Date: October 5, 2013 Time: 7:00 to 8:00 PM

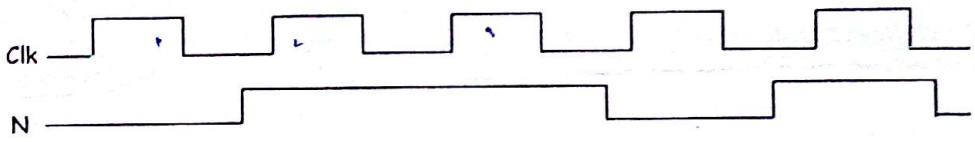
Attempt Any 4 Questions

Q1. a) Design a new positive edge triggered flip flop (say) NP flip flop, starting from a NOR based clocked SR Latch with the condition that if N is equal to P the flip flop output retains the previous value and if N is not equal to P the output takes the value of N. Use any Gates of your choice including Multiplexers. (3)

b) Use the above designed NP flip flop to obtain a T flip flop. (2)

Q2. Draw the timing diagrams, showing the output (M) and the states as a function of time, for the input (N) to the finite state machine whose state diagram is given below. Assume negative edge triggered flip flops are used in this machine. Realize this state machine using one T Flip Flop and one D Flip Flop. (5)

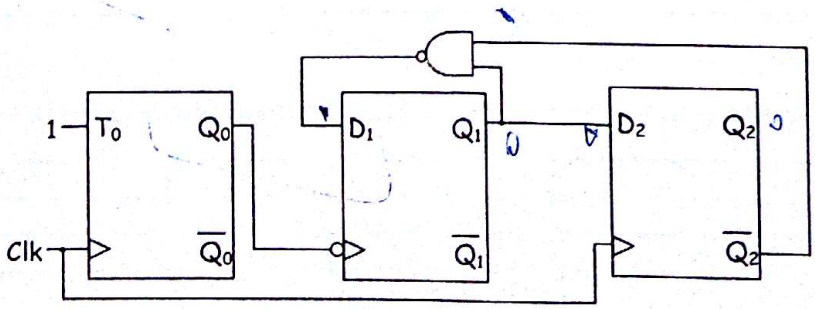




Q3. Using a 1.2MHz. clock, obtain a clock that runs at 200kHz. Note that a clock has a duty cycle of 50% i.e. the time for which the clock stays high is equal to the time for which it stays low in a cycle. For your circuit ensure that it will not get stuck in any lock up state. The FFs do not have direct set and clear. (5)

Q4. Design a sequential circuit using state machine approach with the following function:
The system has one input X (a sequence of bits are input, one bit per clock cycle), an output Z and a clock input. At the first clock edge the output Z equals the input X. Subsequently after every three clock cycles the output gets complement of the maximum occurrence of the last three cycles. (e.g.) in the sequence "010", the maximum occurrence is "0". (5)

Q5. For the circuit shown below, draw the timing diagram (for 4 Clk periods) assuming that at time t = 0, the outputs Q_0, Q_1 and Q_2 are respectively 0, 0, and 0. Assume the flip flop delays are negligible. (5)



Offset binary